CLAIMS

What is claimed is:

1. A memory error management method comprising:

attempting to access information in an error checking and correction memory;

determining if an error exists in the information;

deciding if an error is correctable or not correctable;

engaging in an error correction process; and

performing a memory cell error resolution process.

2. The memory error management method of Claim 1 wherein said information is a plurality of bits in a memory controller buffer cell.

3. The memory error management method of Claim 1 wherein said error checking and correction memory is a memory controller buffer of a disk array memory system.

4. The memory error management method of Claim 1 wherein said error correction process is a single bit error correction code process that corrects a single bit error inline.

5. The memory error management method of Claim 1 wherein a hamming code and error syndrome is utilized to correct a bit in error.

6. The memory error management method of Claim 1 wherein said memory cell error resolution process includes rewriting information to a memory control buffer location.

7. The memory error management method of Claim 1 wherein said memory cell error resolution process includes rewriting corrected information to a memory controller buffer location and if said rewriting resolves the error a soft correctable error count is incremented.

8. The memory error management method of Claim 1 wherein said memory cell error resolution process includes a memory controller fail over process in which an alternate memory controller buffer takes over master responsibilities associated with an overall memory input/output operation.

9. A memory controller comprising:

a communication bus for communicating information between components of said memory controller;

a controller processing core for directing operations of said memory controller and providing a platform to implement a memory error management process, said controller coupled to said communication bus;

an XOR array for providing correction of single bit errors, said XOR array coupled to said communications bus;

a memory controller buffer for storing information being communicated by said memory controller between a host and a physical memory medium, said controller buffer coupled to said XOR array;

a backend interface for providing a communications interface to back end components, said backend interface coupled to said communications bus; and

a front end interface for providing a communications interface to front end components, said front end interface coupled to said communications bus.

10. A memory controller of Claim 9 wherein an error is detected at a location within said memory controller buffer and said controller processing core directs rewriting information to said location and rechecking for an error in said location.

11. A memory controller of Claim 10 wherein said controller processing core directs a reread of information from a physical memory medium and the reread information is utilized in said rewrite to said location.

12. A memory controller of Claim 10 wherein said controller processing core fences off said location and rewrites said information to a different location within said memory controller buffer.

13. A memory controller of Claim 9 wherein an error is detected and said controller processing core relinquishes responsibility for master control operations to an alternate memory controller.

14. A memory controller of Claim 13 wherein an overall memory input/output operation that resulted in said error is treated as not complete and said processing core relinquishes responsibility for master control operations to an alternate memory controller that completes said overall memory input/output operation

15. A memory controller of Claim 9 wherein said controller processing core receives responsibility for master control operations from another memory controller and processes a memory input/output operation request that produced an unrecoverable error.

16. A memory controller of Claim 9 further comprising an accumulator for storing information associated with the logic and arithmetic operations of said XOR array, said accumulator coupled to said XOR array.

17. The memory controller of Claim 7 wherein said controller processing core directs tracking of error information including counts of soft correctable errors, hard correctable errors and non-correctable errors.

18. A memory error resolution process comprising:

receiving information indicating whether an error is a correctable error or a non-correctable error;

performing a memory controller buffer refreshing process;

engaging in a correctable error handling process; and

performing a non-correctable error handling process.

19. A memory error resolution process of Claim 18 wherein said memory controller buffer refreshing process comprises re-entering corrected information into said memory controller buffer location.

20. A memory error resolution process of Claim 19 wherein a soft correctable error handling process is engaged if no errors exist after said re-checking information in said memory controller buffer.

21. A memory error resolution process of Claim 20 wherein a soft correctable error handling process comprises tracking soft correctable error information including incrementing a soft error correctable count.

22. A memory error resolution process of Claim 19 wherein a hard correctable error handling process is implemented if an errors exist after said re-checking information in said memory controller buffer, said hard correctable error handling process includes an error fail-over process that utilizes resources of a different or alternate memory controller buffer

22. A memory error resolution process of Claim 19 wherein said non correctable error handling process comprises:

fencing off of a memory controller buffer location; and

forwarding the information to another location within a memory controller buffer.

23. A memory error resolution process of Claim 19 wherein said non-correctable error handling process comprises an error fail-over process in which an initial memory controller that had control when a memory I/O operation resulted in a memory error relinquishes control to an alternate memory controller and said alternate memory controller attempts to complete said memory I/O operation.

24. A memory error resolution process of Claim 18 further comprising performing a recursive error handling process.

25. A memory error resolution process of Claim 18 further comprising

performing a predictive failure analysis process.